Coupled Electromagnetic-Circuit Simulation of Arbitrarily-Shaped Conducting Structures

Yong Wang, Vikram Jandhyala, and C.-J. Richard Shi
Dept. of Electrical Engineering, University of Washington, Seattle, WA 98195
Phone: (206)-221-5720 Fax: (206)-543-3842 Email: {yongw, jandhyala, cjshi}@ee.washington.edu

Abstract–This paper presents a triangular surface mesh-based formulation of the Partial Element Equivalent Circuit (PEEC) approach. Rao-Wilton-Glisson (RWG) basis functions defined on triangular tessellations are used to model arbitrarily-shaped conducting structures via SPICE compatible netlists. This approach is potentially useful for modeling on-chip electromagnetic interactions.

I. INTRODUCTION

The PEEC method [1] is a particularly effective approach for modeling the electromagnetic effects of a multi-wire or multi-conductor structure using SPICE compatible elements. The classical PEEC method relies on a longitudinal filament discretization of all structures. This paradigm, which assumes a direction of current flow along the length of the filament, is well-suited for thin and long interconnect structures. A System-on-Chip (SoC) scenario [2], however, involves some arbitrarily shaped structures, including inductors, regular and split ground planes wherein the filament approach is inherently not well suited, because of the arbitrary directions of current flow in such structures.

In this paper, we utilize Rao-Wilton-Glisson (RWG) basis functions [3,4], which are linear basis functions defined over triangles, to model conductors using surface triangular meshes [5]. Interactions between RWG basis functions are then represented as circuit elements, in a manner analogous to that used in the classic filament-based PEEC approach. This surface-only formulation includes a surface-impedance term to represent high-frequency skin effects and should prove to be valuable for modeling conducting structures in SoC scenarios.

II. TRIANGULAR MESHES AND PARTIAL ELEMENT EQUIVALENT CIRCUIT EXTRACTION

A typical electromagnetic problem involving three-dimensional multi-wire or multi-conductor structures can be described using the Electric Field Integral Equation (EFIE) [3]. In the EFIE formulation, the unknowns are scalar potential φ, surface charge density ρ and current density $\overline{J}$. Note the explicit use of potential as an unknown for low-frequency stability and compatibility with circuit-level voltages. The resulting EFIE is

$$j\omega \frac{\mu}{4\pi} \int_S \frac{\overline{\mathbf{J}}(\mathbf{r}')}{|\mathbf{r}-\mathbf{r}'|} ds' + (\nabla \varphi)(\mathbf{r}) = -R\,\overline{\mathbf{J}}(\mathbf{r}) \tag{1}$$

$$\varphi = \frac{1}{4\pi\varepsilon} \int_S \frac{\rho(\mathbf{r}')}{|\mathbf{r}-\mathbf{r}'|} ds' \tag{2}$$

where R is the surface resistance for non-ideal conductors and is given by $\mathrm{R} = \mathrm{Re}\left(\sqrt{\frac{j\omega\mu}{2\sigma}}\right)$ and σ is the volume conductivity.

Assuming a triangular tessellation of the conductor surfaces with N_e non-boundary edges and N_p patches, Eqns. (1) and (2) can be recast as

$$j\omega \overline{\mathbf{L}}\mathbf{I} + \overline{\mathbf{A}}\varphi = \overline{\mathbf{R}}\mathbf{I} \tag{3}$$

$$\overline{\mathbf{P}}\,\mathbf{Q} = \mathbf{V} \tag{4}$$

where $L_{ij} = \frac{\mu}{4\pi} \int_S \int_S \frac{\mathbf{f}_j(\mathbf{r}')}{|\mathbf{r}-\mathbf{r}'|} ds' \cdot \mathbf{f}_i(\mathbf{r}')\, ds \quad i, j = 1,..,N_e$, with $\mathbf{f}$ denoting an RWG basis function, $\overline{\mathbf{A}}$ is a sparse coefficient matrix with two non-zero elements at each row, $P_{ij} = \frac{1}{4\pi\varepsilon} \int_S \int_S \frac{\nabla' \cdot \mathbf{f}_j(\mathbf{r}')}{|\mathbf{r}-\mathbf{r}'|} \nabla \cdot \mathbf{f}_i(r)\, ds\, ds' \quad i, j = 1,\ldots,N_p$, and $\overline{R}$ is a sparse, nearly diagonal matrix, with $R_{ij} = R \int \mathbf{f}_i(\mathbf{r}) \cdot \mathbf{f}_j(\mathbf{r})\, ds$ if edge i and edge j share a common triangle, and 0 otherwise.

As in the classic filament-based PEEC method, mutual capacitances and inductances can be obtained through Voltage Controlled Voltage Sources (VCVSs) available in SPICE. For example, using the relation $j\omega L_{ij} I_j = L_{ij}(j\omega I_j) = L_{ij} \frac{\varphi_{jj}}{L_{..}}$,

0-7803-7024-4/01/$10.00 © 2001 IEEE

mutual inductance can be represented by a VCVS. Off-diagonal R_{ij} entries are represented by Current Controlled Voltage Sources. The triangular mesh-based circuit topology is shown in Fig. 1, and a typical PEEC cell is shown in Fig. 2.

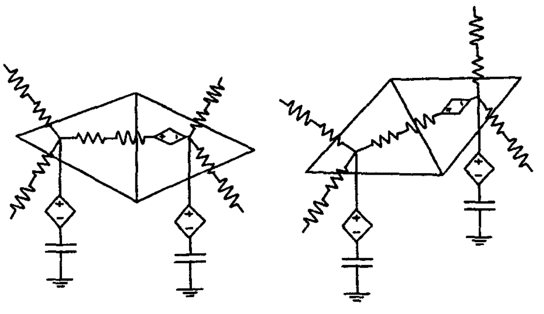


Figure 1. PEEC elements defined on triangular meshes.

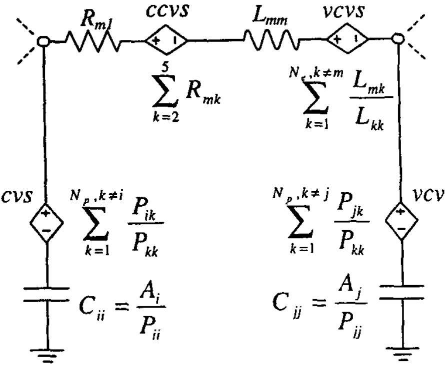
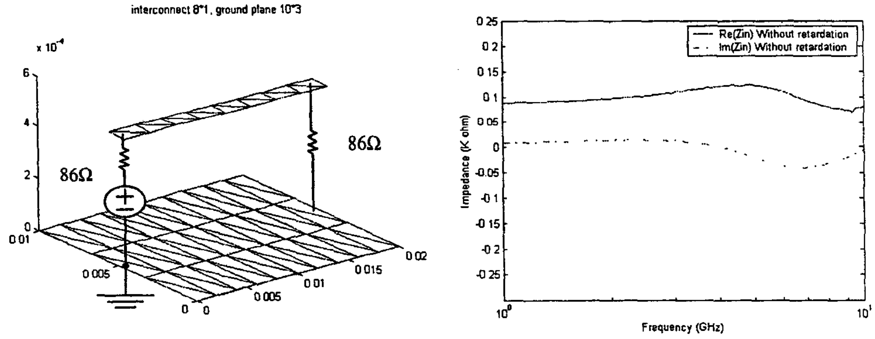


Figure 2. A typical PEEC cell.

III. NUMERICAL RESULTS

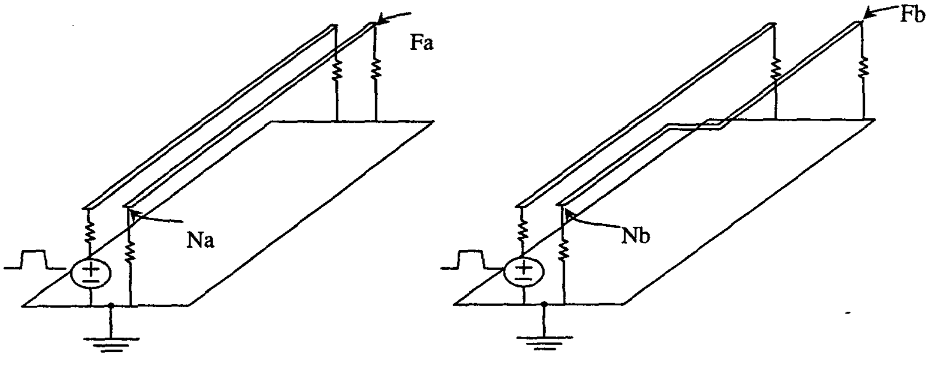
The first example, depicted in Fig. 3, is an interconnect over a ground plane, and is used to validate the triangular approach against the previously published filament PEEC solution [6]. The interconnect is driven by a voltage source and is terminated by 86 Ohm resistors at both ends. The ground plane is 2.0cm long by 1.0cm wide. The interconnect is 2.0cm long, 1mm wide and 0.5mm above the ground plane. The input impedance shown in Fig. 3 (b) matches very well with the published filament PEEC result [6].



(a) (b)

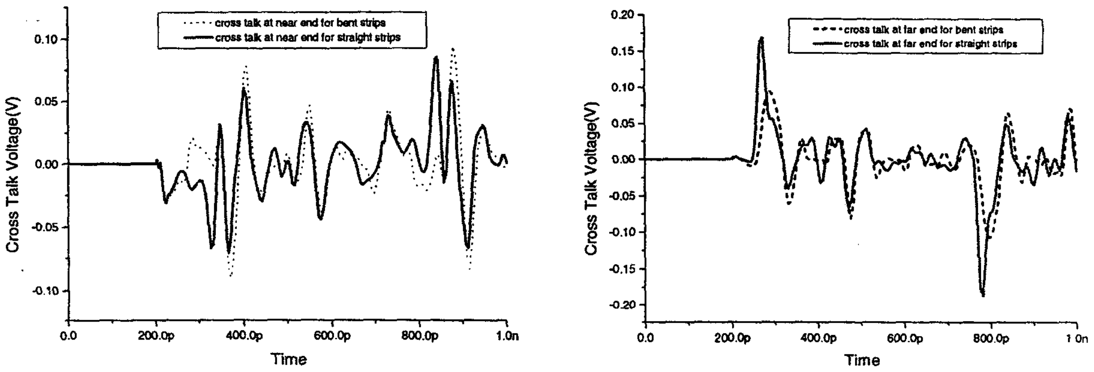
Figure 3. (a) Triangular discretization of the strip and the ground plane. (b) Input impedance of active line.

The second example illustrates the use of the triangle-based PEEC for time-domain cross-talk analysis. We consider two scenarios as shown in Fig. 4; in one scenario two strips are 0.5mm above the ground plane and 1mm apart, and in the other the two strips are also 0.5mm above the ground plane and 1mm apart at the near end, but 3mm apart at the far end. When a pulse input is added at one strip, the cross-talk voltages can be observed via a triangle-based PEEC time-domain simulation, as shown in Fig. 5. The simulation results show that the wider separation results in a smaller cross talk voltage.



(a) (b)

Figure 4. (a) Two parallel strips. (b) Two strips, with larger distance at the far end.



(a) (b)

Figure 5. (a) Cross talk at the near end. (b) Cross talk at the far end.

The third example is a spiral inductor, of dimensions 200μm×200μm and 30μm above the ground plane, as illustrated in Fig. 6. The line width and the gap width of the inductor are both 20μm.

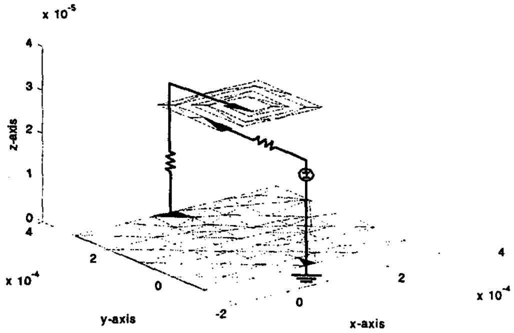
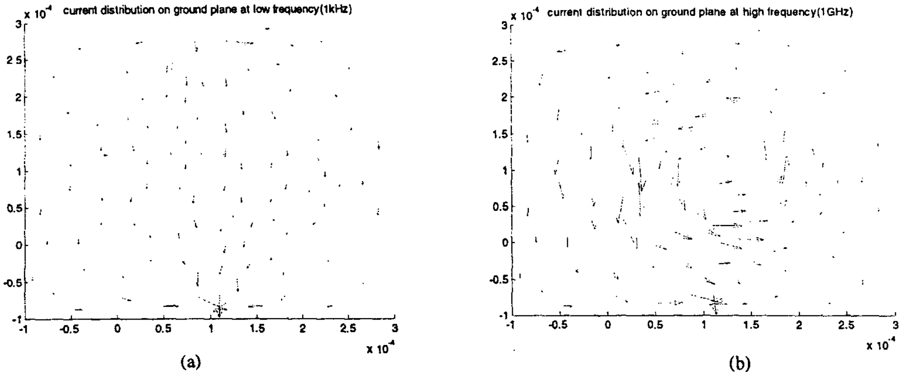


Figure 6. Spiral inductor above a ground plane.

The triangular PEEC approach is used to model the induced current distribution on the ground plane at both low and high frequencies, 1KHz and 1GHz respectively. The results of triangle PEEC simulation are given in Figs. 7(a) and 7(b). The physically correct behavior associated with low- and high- frequency induced currents is reproduced: while the currents are spread out over the ground plane at lower frequencies, the increased inductive component of impedance at higher frequencies dictates that the induced current crowd under the inductor. This phenomenon is modeled very accurately with the triangular discretization. It is expected that this ability to model true current distributions will make the triangular PEEC method particularly suited for SoC applications.



(a) (b)

Figure 7. (a) Low frequency ground plane current distribution (1KHz). (b) High frequency ground plane current distribution (1GHz).

IV. CONCLUSIONS

A modified PEEC approach based on triangular tessellations on surface meshes was presented. The resulting partial capacitance, inductance, and surface resistance terms were used to obtain an equivalent SPICE model. Numerical results were presented to validate the approach and demonstrate its advantages in modeling induced and return current densities. The approach also has the advantage of modeling thin structures with a two-dimensional formulation. It is expected that a hybrid approach, with filaments to model current flow on longitudinal interconnects, and triangles to model arbitrarily-shaped structures and ground planes will yield the best results in terms of accuracy and efficiency. Future work will aim at enhancements to the triangle-based formulation including a full-wave time domain implementation, a fast matrix-vector multiply scheme, and reduced-order modeling.

This work was supported in part by the Defense Advanced Research Projects Agency under the NeoCAD initiative, in part by the National Science Foundation and the Semiconductor Research Corporation under a joint initiative on Mixed-Signal Electronic Technologies, and in part by by NSF CAREER grant ECS-0093102.

REFERENCES

[1] A. E. Ruehli, "Equivalent circuit models for three-dimensional multiconductor systems," *IEEE Trans. on Microwave. Theory and Techniques.*, vol. MTT22 (3), pp. 216-221, March 1974.

[2] K. Kundert, H. Chang, D. Jefferies, G. Lamant, E. Malavasi, and F. Sendig, "Design of mixed-signal systems-on-a-chip," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19 no.12, pp. 1561–1571, Dec. 2000.

[3] Andrew F. Peterson, Scott L. Ray, Raj Mittra, *Computational Methods for Electromagnetics*, IEEE PRESS, 1997.

[4] S. M. Rao, D. R. Wilton, and A. W. Glisson, "Electromagnetic scattering by surfaces of arbitrary shape," *IEEE Trans. Antennas Propagation*, vol. AP-30, pp. 409-418, May 1982.

[5] Coen, G., Fache, N., de Zutter, D., Lagasse, P. "Automatic equivalent discrete distributed circuit generation for microstrip interconnection discontinuities," *Proc. Antennas and Propagation Society International Symposium*, 1994. AP-S. Digest , Volume: 3, pp1702 -1705, 1994.

[6] W. Pinello, A. C. Cangellaris, and A. Ruehli, "Hybrid electromagnetic modeling of noise interactions in packaged electronics based on the partial-element equivalent-circuit formulation," *IEEE Trans. on Microwave Theory and Techniques*, vol. 45, no.10 part 2, pp. 1889–1896, Oct. 1997.