

Including the Impact of Connecting Vias in the Performance Metric Evaluation for Board-Level Optimization of Decoupling Capacitors

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Abstract: Existing decoupling capacitor optimization techniques tend to neglect the impact of via parasitics while evaluating the performance metrics. This work demonstrates that ignoring the impact of connecting vias can produce optimistic results leading to functional failure. An efficient method for including via-parasitics in the performance metric evaluation is presented for more accurate design optimization.

1. Introduction

Automatic placement of decoupling capacitors in a power delivery network (PDN) to meet specified constraints while minimizing cost is an important design automation goal. The problem can be formulated as a combinatorial optimization problem where a number of decoupling capacitors are to be chosen from a set of capacitors and placed at desired locations out of the factorially large number of possible locations so as to meet the design goal at the lowest cost. For this kind of combinatorial optimization, simulated annealing has been the choice of many past works [1, 2]. Use of fast methods for evaluating the objective function is a primary requirement for practical use of any optimization tool. In [1], resistance-capacitance-susceptance macromodel is generated by model order reduction with ports defined at the possible capacitor locations and simulated annealing based optimization is performed to maintain the impedance below a target value over a given frequency range. It is well known that the parasitic components of the decoupling capacitors, namely ESL and ESR, play vital role in determining the effectiveness of the capacitors for decoupling. In [2], the method of [1] is modified to incorporate the effect of ESR and ESL for better accuracy. The switching current appearing in a PDN may not have components in the entire frequency range under consideration. Thus, maintaining an upper bound of the impedance over the entire frequency range may lead to overdesign. This fact is demonstrated in [2] and target noise voltage, rather than target impedance is considered as the metric which yields more optimized decoupling. Both [1, 2] target package-level optimization and ignore the impact of the vias that connect the decoupling capacitors to the power planes. While evaluating performance metrics for board-level designs, ignoring the via-parasitics may lead to underestimation of the impedance or noise metric since the connectors can be considerably long in the board level.

The aim of this paper is to provide a method for accurate performance metric evaluation for use within an optimization framework. However, implementation of any particular optimization method is beyond the scope of this paper. It is demonstrated that the evaluation of performance metrics without considering the impact of connecting vias can be optimistic. Since the partial mutual inductance between the vias change with the location of the decoupling capacitors, the parasitics of the vias cannot be represented by effective series elements. Therefore, an algorithm is presented for including the parasitics of the connecting vias in the performance metric evaluation routine. An efficient implementation of the multilayer finite difference method (MFDM) has been made in this work for fast macromodel generation and quick design iterations.

3. Impact of Ignoring Via-to-Via Interaction

The impact of ignoring via-parasitics during the performance metric evaluation is demonstrated with the testcase shown in Figure 1, similar to the design originally considered in [2]. Two 0.025mm (1mil) thick copper planes, 20mm × 10mm (800mil × 400mil), are separated by 0.25mm (10mil) FR4 dielectric material with dielectric constant 4.0 and loss tangent 0.02. The IC chip is lying along the long edge, as shown in the figure. Due to two triangular current pulses with peak magnitude of 250mA and rise/fall time 100ps applied at the left and right port, the impedance and noise voltage are evaluated at the middle port with and without considering the connecting vias. The vias are 0.254mm (10mil) in diameter. Figure 2 shows the

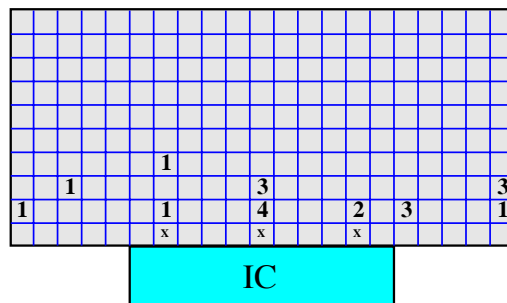


Figure 1: Example design similar to the design presented in [2]. Decoupling capacitor locations are shown in the grid by numbers where 1,2,3,4 represent types of capacitors [1, 2]. Cross marks indicate the port locations.

transfer impedance between the left and middle ports with and without considering the vias. Above 50MHz, neglecting the via-parasitics makes the transfer impedance almost four times less than the actual impedance obtained with the via parasitics. Additionally, without modeling the connecting vias, the transfer impedance reaches its first peak of 5.16Ω at 4.4GHz instead of the actual peak value of 47.08Ω occurring at 2.8GHz. The effect of this difference in impedance will be visible in the time domain simulation of noise at the middle port, as depicted in Figure 3. When the connecting vias are not modeled, for a voltage supply of 2.5V and a tolerance of 20% (0.5V), the design may appear to be “optimized” since the peak noise is 0.5V. However, with the vias modeled, the waveform shown in Figure 3 shows a peak voltage of 1.2V, which is clearly unacceptable. Therefore, the “optimal” result obtained without modeling the vias can be far from being optimal, both for impedance (frequency domain) and noise (time domain) targets. Moreover, the impact of via parasitics on the decoupling behavior will increase with via-length and, thus, will be more prominent for a thicker power bus or a power bus embedded deeper in a board.

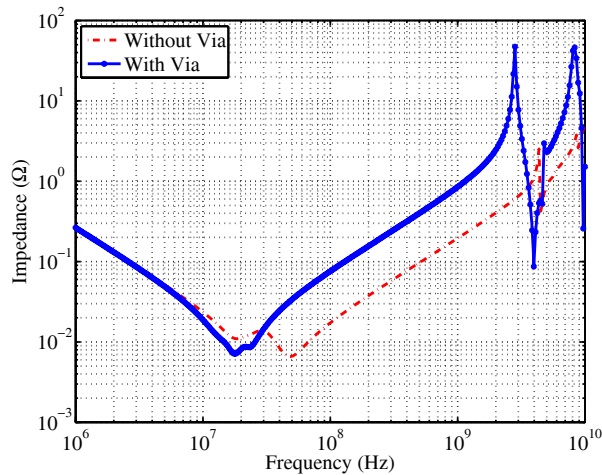


Figure 2: Transfer impedance as a function of frequency between the left and the middle ports of Figure 1.

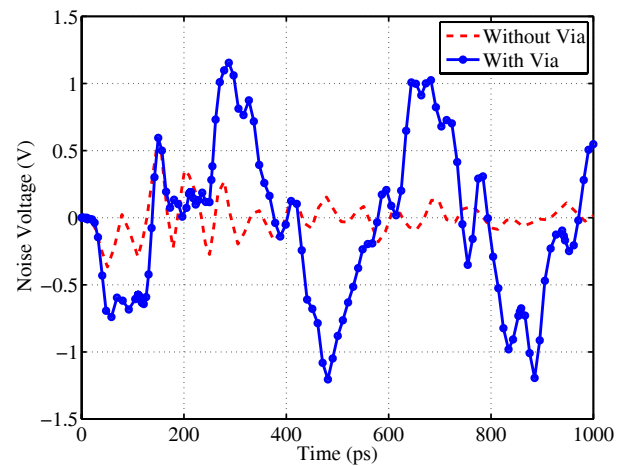


Figure 3: Noise voltage as a function of time appearing at the middle port due to current pulses in the left and right ports.

3. Generation of Macromodel for the Power Bus

Board-level optimization of decoupling capacitors using full model of the power bus will be inefficient since the time required for performance metric evaluation will be long. Therefore, use of macromodel is common for this kind of optimization. In [1, 2], the macromodels are generated by model order reduction of large resistance-inductance/susceptance-capacitance model obtained by extraction. Although accurate, such methods are not amenable to design space exploration and design iteration. For example, the thickness of the power bus determines the effectiveness of local decoupling [3]. Therefore, changing the thickness of the bus can be part of the overall board-level design optimization. A more efficient method will be useful.

The multilayered finite difference method [4] is adopted for this work since the technique has good accuracy and can be implemented efficiently. A cell-centered 5-point discretization scheme is adopted in this work. The design is divided into small square cells and the per-unit-cell resistance-inductance-conductance-capacitance (RLGC) parameters are estimated using simple quasi-static expressions. The formulation of the method can handle wrap-around currents for multilayered designs [4]. By defining nodes at the center of each cell, a sparse admittance matrix (\mathbf{Y}) is derived. Solving the equations $\mathbf{YV} = \mathbf{I}$ for voltage, frequency dependent impedance is obtained for specified locations. For generating the macromodel, ports need to be defined at the desired locations.

The sparsity of the admittance matrix can be exploited for enhancing the efficiency of the solver. In fact, a SPICE netlist can be easily generated and solved using simulators like HSPICE. However, using a sparse matrix solver will be much more advantageous, particularly for large complex designs. For this work, the sequential version of the sparse matrix package SuperLU [5] is used for solving the system of equations. For a medium sized problem with 22500 nodes, this particular implementation is 70X faster than HSPICE. For larger models, the difference will be even more significant.

4. Inclusion of Via-to-Via Interaction

As described in the previous section, the analysis of the PDN is based on the admittance matrix formulation. Therefore, for the evaluation of impedance after inserting the decoupling capacitors, the macromodel for the original model (without any decoupling capacitors and port vias) is represented in terms of the admittance parameters. A decoupling capacitor is inserted between a pair of nodes in the macromodel using two connecting vias. Before describing

the method of forming the admittance matrix for the structure with the decoupling capacitors, estimation of the via-parasitics, namely the resistance and partial inductance [6], is discussed.

Figure 4 shows how the capacitors and the IC power pins are connected to the macromodel through vias. Each via has some resistance, partial self inductance and is coupled with the rest of the vias through partial mutual inductances. The resistance of a via can be determined by the simple formula $\rho l/A$ where ρ is the resistivity of the material of via, l is the length of the via and A is the effective cross section of the via. The partial self and mutual inductance of each via is determined as the inductance with current returning at infinity [6]. When the whole circuit is solved using the admittance matrix, which has the connectivity information in it, the return paths are automatically determined and inductance loops are closed to yield the physically meaningful loop inductance. Since the vias may connect to different planes, their whole lengths may not interact with each other. Therefore, only the common length between each pair of vias needs to be considered for computing partial mutual inductance between them. As confirmed by measurements [7], the partial mutual inductance formula presented in [8] is accurate for via structures found in PCBs:

$$M_{ij} = \frac{\mu_0 l}{2\pi} \left[\ln \left(\frac{l}{d} + \sqrt{1 + \frac{l^2}{d^2}} \right) - \sqrt{1 + \frac{d^2}{l^2}} + \frac{d}{l} \right] \dots (1)$$

where M_{ij} is the partial mutual inductance between via i and j , μ_0 is the permeability of free space, l is the length common to the two vias, and d is the center to center distance between the vias. The partial self inductance of a via can be found as the summation of the partial mutual inductance between two identical filaments separated by distance equal to the radius of the via and the internal inductance [7]. Alternative curve fitted formulae have been presented in [9] where the self and mutual inductances are derived considering the fact that currents return only through the region limited by the power bus. The expressions in [9], thus, contain the dimensions of the power bus as well.

Once the parasitic components of the vias are found, the admittance matrix $Y(\omega)$ is to be constructed, where ω is the angular frequency. Let us assume that there are n nodes in the macromodel and the corresponding admittance matrix is $Y_{macro}(\omega)$. Two vias are connected for each decoupling capacitor and input/output port. Each via has one end connected to a macromodel node, or to the “ground” node, while new nodes are formed at the other end. For example, when the first capacitor is connected between nodes N_i and N_j of the macromodel through vias, the first via is connected between N_i and a newly formed node N_{n+1} , whereas the second via is connected between N_j and newly formed node N_{n+2} . The capacitor along with its ESR and ESL actually appears in between nodes N_{n+1} and N_{n+2} . If the total number of decoupling capacitors and input/output ports is m , then the total number of nodes in the new system represented by $Y(\omega)$ will be $n+2m$.

Initially, the admittance values in $Y(\omega)$ corresponding to the nodes of the macromodel are copied from $Y_{macro}(\omega)$, some of which will be modified due to their connection to the vias. The series impedance of each decoupling capacitor excluding the vias will be $Z_d = (ESR + j\omega ESL + 1/j\omega C)$, where C is the value of the capacitors and ESL/ESR bears the usual meaning. If the capacitor is connected between node i and j , then the elements of the $Y(\omega)$ matrix will be updated to, in MATLAB notation, $Y(i,i) = Y(j,j) = 1/Z_d$ and $Y(i,j) = Y(j,i) = -1/Z_d$.

To update $Y(\omega)$ with admittance values due to partial inductance and resistance of the via connections, first a complex impedance matrix is formed. This is illustrated for the simple case of two vias interacting with each other and then extended to the general case. Figure 5 shows two coupled vias that connect a capacitor to the macromodel. The node voltages are V_1 through V_4 for nodes N_1 through N_4 . The currents, entering into the vias, are I_1 through I_4 . With $I_1 = -I_3$ and $I_2 = -I_4$, the nodal equations are given by:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & j\omega M \\ j\omega M & R_2 + j\omega L_2 \end{bmatrix}^{-1} \begin{bmatrix} V_1 - V_3 \\ V_2 - V_4 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 - V_3 \\ V_2 - V_4 \end{bmatrix} \dots (2)$$

The overall current equations, therefore, will be:

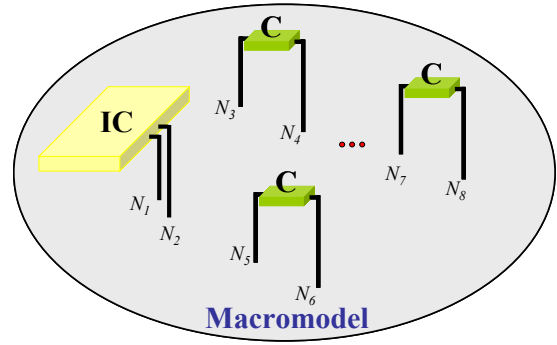


Figure 4: Connection of decoupling capacitors and IC power pins with the power bus macromodel using connecting vias.

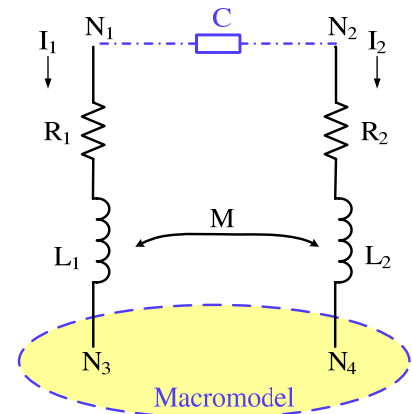


Figure 5: Inductive coupling between two vias connecting a capacitor to the macromodel.

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & -Y_{11} & -Y_{12} \\ Y_{12} & Y_{22} & -Y_{12} & -Y_{22} \\ -Y_{11} & -Y_{12} & Y_{11} & Y_{12} \\ -Y_{12} & -Y_{22} & Y_{12} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \dots (3)$$

The admittance values from (3) will be added to the appropriate entries in the $\mathbf{Y}(\omega)$ matrix constructed so far. In case N_3 or N_4 represents the “ground” node, the corresponding voltage could be omitted from (3).

In the general case of k vias interacting with each other, the $k \times k$ impedance matrix, $\mathbf{Z}(\omega)$ will be constructed with $Z(i,i) = (R_i + j\omega L_i)$ and $Z(i,j) = j\omega M_{ij}$. Inverting the matrix $\mathbf{Z}(\omega)$, the admittance parameters between the nodes of the vias not connected to the macromodel (N_1, N_2 in Figure 5, for example) will be obtained, as in case of (2). The nodes of the vias those are connected to the macromodel, such as N_3, N_4 in Figure 5, can be handled in the same way (3) is derived. It may appear that the cost of inverting the $k \times k$ matrix $\mathbf{Z}(\omega)$ will be a limiting factor since inversion is an $O(n^3)$ operation, but the number of decoupling capacitors will seldom exceed 100 for which the inversion operation can be performed in less than 10ms on any modern computer. To verify the accuracy of the method for constructing the admittance matrix, the testcase of Figure 1 including the vias is modeled with resistance-inductance-capacitance in HSPICE. In Figure 6, the self impedance of the middle port and the transfer impedance between the left and the middle port are plotted. HSPICE results match exactly with the results of the proposed method validating its accuracy.

5. Conclusions

In this paper, it was demonstrated that ignoring the impact of connecting vias can produce unacceptable results for board-level decoupling capacitor optimization. For more accurate performance metric evaluation, a technique for including the parasitics of the connecting vias was presented, which will make the design optimization more accurate. An efficient implementation of the multilayered finite difference method (MFDM) was made for fast macromodel generation that can be used by any optimization method. An optimization flow designed around this framework will enable better exploration of the design space producing better design in reasonable time.

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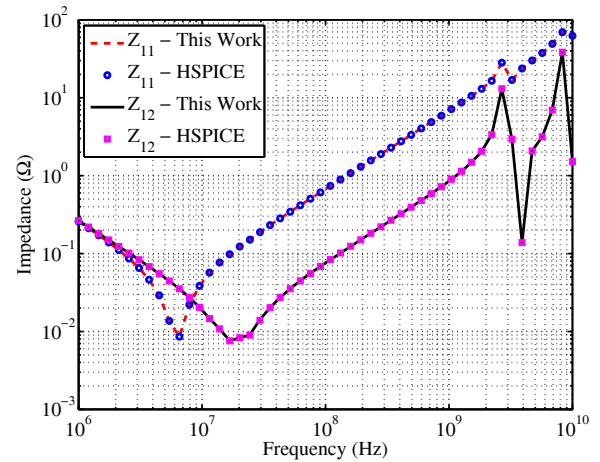


Figure 6: Comparison of results obtained from the proposed method with HSPICE simulation results.